SPECIFICATION

BE IT KNOWN THAT I, KEIKO MIYAJIMA residing at c/o NEW JAPAN RADIO CO., LTD., KAWAGOE SEISAKUSHO, 1-1, Fukuoka 2-chome, Kamifukuoka-shi, Saitama-ken, Japan, a subject of Japan, have invented certain new and useful improvements in

EXTERNAL OUTPUT VIDEO SIGNAL PROCESSOR

of which the following is a specification:-

EXTERNAL OUTPUT VIDEO SIGNAL PROCESSOR

BACKGROUND OF THE INVENTION

This invention relates to an external output video signal processor for carrying out external output of the video signal with a predetermined p-p value. The fundamental configuration of an external output video signal processor currently used conventionally is shown in Fig. 3. The DC component of a video signal output from system controller 10 is cut with coupling capacitor 30. The video signal is taken into clamping circuit 23 (for example, see Japanese Unexamined Patent Publication No. 46443/1995) of video signal processing circuit 20a which consists of a microchip and it's continuous current is regenerated. It is sent to latter part processing circuit 22, and is amplified (p-p value) in the part. After being adjusted, it is output outside. Since the video signal which is output from latter part processing circuit 22 is determined to set to 1.0 Vpp when it is terminated by 75-ohm resistance, the output swing (p-p value) usually serves as 2.0 Vpp.

Fig. 4 is a figure showing the configuration of an external output video signal processor in which system controller 10a of Fig. 3 is shown in more detail. The video signal output by DSP 11 of system controller 10a in current is converted into voltage by resistance 12, matched with impedance by impedance conversion circuit 13, and input into coupling capacitor 30.

If video signal is made to input into latter part processing circuit 22 of video signal processing circuit 20a as it is when the reference level of video signal output from system controller 10a is not

being fixed, or when sync. tip is not the optimal level, crushing occurs in the top or the bottom of the signal wave form, which are output from the latter part processing circuit 22, and when the video signal is reproduced, deterioration of image quality will be caused.

Then, in order to prevent distortion of the signal wave form output from this latter part processing circuit 22, coupling capacitor 30 and clamping circuit 23 are formed as mentioned above. With coupling capacitor 30, DC component of output is cut and only the Alternating Current component is extracted. Continuous current regeneration of this is input and carried out to clamping circuit 23. By doing in this way, sync. tip level and pedestal level are fixed to predetermined level, and the indispensable dynamic range is retained.

SUMMARY OF THE INVENTION

As mentioned above, the conventional external output video signal processor has necessarily equipped coupling capacitor 30 and clamping circuit 23. Even if sync. tip level and pedestal level of video signal output from system controller 10a are in a normal level, it has also coupling capacitor and clamping circuit.

However, when coupling capacitor 30 is used as mentioned above, a high pass filter is constituted by this coupling capacitor 30 and the input impedance of clamping circuit 23. Therefore, when the capacity of coupling capacitor 30 is reduced, there is the problem that shrinkage of synchronizing signal and sag (inclination of top part) will occur. The capacity of coupling capacitor 30 cannot be small for these reasons. Therefore, coupling capacitor 30 could not be built in video signal processing circuit 20a which is a microchip, but there was the

problem of an external output video signal processor that the number of components increased constitutionally.

The object of the invention is offering an external output video signal processor which does not need a coupling capacitor or a clamping circuit, when the sync. tip level and the pedestal level of the video signal which are output from the system controller are in a predetermined level.

In an external output video signal processor which consists of a system controller which outputs a video signal to a video signal processing circuit, and the video signal processing circuit which has a latter part processing circuit, which outputs a video signal of which the p-p value is controlled to a predetermined level, said system controller outputs a video signal by which the sync. tip level and the pedestal level are fixed to a predetermined value. It is considered as an external output video signal processor which carries out direct input of said video signal output to said video signal processing circuit from said system controller, and is characterized by providing a level shift circuit which adjusts the level and is sent to said latter part processing circuit.

Said level shift circuit is constituted by two steps of inversion amplifiers in an external output video signal processor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an external output video signal processor of one embodiment of the invention.

Fig. 2 is a circuit diagram of a level shift circuit of the external output video signal processor of Fig. 1.

Fig. 3 is a block diagram of an external output video signal

processor of the conventional embodiment.

Fig. 4 is a more detailed block diagram of the external output video signal processor of Fig. 3.

DETAILED DESCRIPTION

Fig. 1 is a block diagram showing the configuration of an external output video signal processor of one embodiment of the invention. System controller 10 provides DSP11 which outputs a video signal with a current signal, and resistance 12 which transforms the current signal into a voltage signal. Video signal processing circuit 20, which consists of a microchip, carries out direct input of the signal level output from system controller 10, and provides level shift circuit 21 shifted to a certain level, and latter part processing circuit 22 to which amplitude (p-p value) outputs a video signal of 2.0 Vpp(s).

At this stage, the video signal, as for, the current output carried out by DSP11 is set to a level predetermined in the sync. tip level or the pedestal level when changed into a voltage signal by resistance 12. That is, as for a video signal of current from DSP11, the sync. tip level and the pedestal level are already being fixed to a predetermined value. Therefore, such a video signal can be directly input to level shift circuit 21 of video signal processing circuit 20, without performing DC component cut and continuous current regeneration. However, in the case the video signal is input into latter part processing circuit 22 as it is, a video signal of an amplitude of 2.0 Vpp(s) cannot be output from the part.

Then, it enables it to output a video signal of an amplitude of 2.0 Vpp(s) from there by inserting level shift circuit 21, and inputting

into latter part processing circuit 22, after adjusting the level of the video signal output from system controller 10.

Fig. 2 is a circuit diagram showing the concrete configuration of level shift circuit 21. This level shift circuit 21 comprises two stages of inverting amplifiers.

The first stage of the inverting amplifier comprises inverting amplifier 211, input resistor 212, feedback resister 213, and source 214 of reference voltage of voltage VR1. The latter stage of the inverting amplifier comprises inverting amplifier 215, input resistor 216, feedback resister 217, and reference voltage source 218 of voltage VR2.

By amplifying the video signal to which the sync. tip level and the pedestal level were fixed in level shift circuit 21 which comprises two stages of inverting amplifiers in this way, the video signal of a predetermined level is generated, it is input into latter part processing circuit 22, and the video signal of an amplitude of 2.0 Vpp(s) is output from there.

Thus, even if it deletes conventionally needed coupling capacitor and clamping circuit, the sync. tip level and the pedestal level are fixed on a predetermined level as usual, and a video signal of a predetermined amplitude value (p-p value) can be made to output from latter part processing circuit 22 in the external output video signal processor of this embodiment.

According to the present invention, as explained above, since a coupling capacitor becomes unnecessary, the number of components can be reduced and, thereby, cost cut and space-saving can be attained. Shrinkage of the synchronizing signal and generating of sag resulting from a coupling capacitor can also be prevented.

It is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present invention. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the scope of the present invention, and the appended claims are intended to cover such modifications and arrangements.